Code No:A109210203 | R09 | SET-1

B.Tech II Year - I Semester Examinations, December 2011
ELECTRONIC DEVICES AND CIRCUITS
(COMMON TO EEE, ECE, CSE, EIE, BME, IT, MCT, E.COMP.E, ETM, ICE)
Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) What is Fermi level? By indicating the position of Fermi level in intrinsic, n-type and p- type semiconductor, explain its significance in semiconductors?

b) Sketch V-I characteristics of a PN diode for the following conditions:

i)	$R_f = 0$,	$V\gamma = 0$,	$R_r = \infty$
ii)	$R_f = 0$,	$V\gamma = 0.6V$,	$R_r = \infty$
iii)	$R_f =$ Non-zero, fixed value,	$V\gamma = 0$,	$R_r = \infty$
iv)	$R_f =$ Non-zero, fixed value,	$V\gamma = 0.6V$,	$R_r = \infty$

Where $V\gamma$ is the cut-in voltage, R_f is the forward dynamic resistance & R_r is the reverse dynamic resistance of the diode. [7+8]

2.a) Draw the block diagram of a regulated power supply and explain its operation.

b) A full wave bridge rectifier having load resistance of 100Ω is fed with 220V, 50Hz through a step-down transformer of turns ratio 11:1. Assuming the diodes ideal, find
i) DC output voltage
ii) Peak inverse voltage
iii) Rectifier efficiency. [9+6]

3.a) With a neat diagram explain the various current components in an NPN bipolar junction transistor & hence derive general equation for collector current, I_C?

b) What is Early-effect; explain why it is called as base-width modulation? Discuss its consequences in transistors in detail? [9+6]

4.a) What is 'Thermal Runaway' in transistors? Derive the condition to prevent 'Thermal Runaway' in Bipolar Junction Transistors.

b) A silicon NPN transistor has Ico = 20nA and β=150, V_{be} = 0.7V. It is operated in Common Emitter configuration (as shown in Figure.1) having Vbb = 4.5V,R_b= 150K,R_c = 3K, V_{cc} = 12V. Find the emitter, base and collector currents and also verify in which region does the transistor operate. What will happen if the value of the collector resistance is increased to very high values? [5+10]

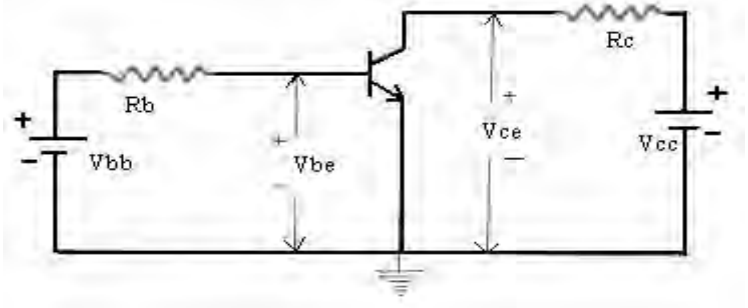

Figure.1

5.a) Draw the circuit diagram & small signal equivalent of CB amplifier using accurate h-parameter model. Derive expressions for A_V, A_I, R_i and R_0.

b) Draw small signal equivalent circuit of Emitter Follower using accurate h-parameter model. For the emitter follower circuit with R_S = 0.5K and R_L = 5K, calculate R_i, A_V and R_O. Assume, h_{fe} = 50, h_{ie} =1K, h_{oe} = 25 μA/V. [8+7]

6.a) Explain the construction & operation of a P-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?

b) "A depletion mode MOSFET can also be operated in enhancement mode but an enhancement mode MOSFET cannot be operated in depletion mode". Justify? [10+5]

7.a) Explain the need of biasing a Field Effect Transistor. With necessary equations and valid reasons explain why a simple 'fixed bias' arrangement for FETs is not used in practical applications?

b) A Common Source FET amplifier circuit shown in Figure.2 with un-bypassed R_S has the following circuit parameters: R_d = 15K, R_S = 0.5K, Rg = 1M, r_d = 5K, g_m= 5mS and V_{DD} = 20 V. Calculate A_V, A_I, R_i and R_0. [7+8]

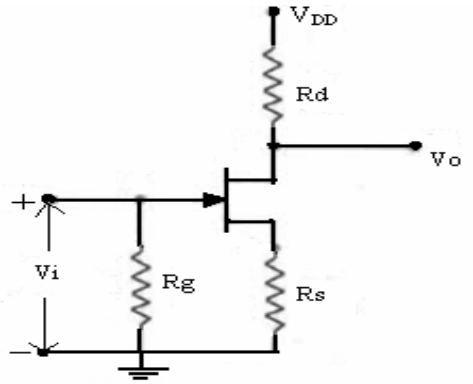

Figure.2

8.a) With neat energy band diagrams, explain the V-I characteristics of Tunnel diode. Also discuss the negative resistance property of tunnel diode.

b) With neat sketches explain the operation of Schottky Barrier Diode. [10+5]

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Answer any five questions
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1.a) What do you understand about the depletion region at a PN junction, with the help of necessary diagrams and derive expression for barrier potential.
b) Derive the expression for transition capacitance, C_T of a PN diode. [9+6]

2.a) With neat sketches explain the operation of a FWR with L- section filter & derive the expression for its ripple factor. Also explain the necessity of a bleeder resistor in a practical L- section filter.
b) Determine the ripple factor of an L-section filter comprising a 10H choke and 8μF capacitor, used with a FWR. The DC voltage at the load is 50V. Assume the line frequency as 50Hz. [10+5]

3.a) Draw the circuit diagram of NPN transistor in Common Emitter(CE) configuration. With neat sketches and necessary equations, describe its static input-output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?
b) Calculate the values of I_C and I_E for a transistor with α_{dc} = 0.99 and I_{CBO} = 5μA, if I_B is measured as 20 μA. [10+5]

4.a) What do you mean by biasing a transistor? Explain the need of biasing a transistor for the construction of a faithful amplifier?
b) Design a collector to base bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50. [7+8]

5.a) In the amplifier circuit shown in Figure.1, estimate input resistance and voltage gain? Also derive the expressions used?

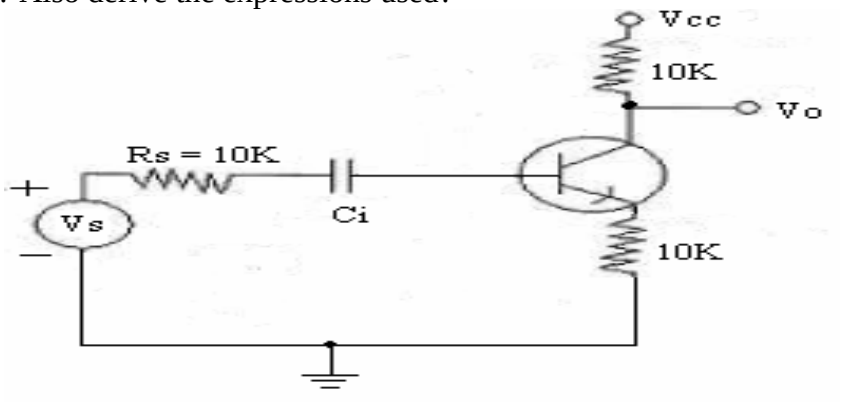

Figure.1

b) Compare CB, CE and CC amplifiers with respect to A_V, A_I, R_I & R_O? [10+5]

6.a) Explain the construction & operation of a P-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?

b) In an n-channel FET, the effective channel width is $3x\ 10^{-4}$cm and the donor impurity concentration is 10^{15} electrons/cm^3. Find the pinch-off voltage? [10+5]

7.a) Draw the basic circuit and small-signal model of Common Drain FET amplifier. Derive expressions for voltage gain and output resistance?

b) Compare the merits & demerits of a Bipolar Junction Transistor (BJT) with Field effect Transistor (FET) in detail? [8+7]

8.a) Draw the firing characteristics of SCR and briefly explain it.

b) Define the following with respect to SCR

i) Forward break over voltage

ii) Reverse break over voltage

iii) Holding current

iv) Gate trigger current. [7+8]

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Answer any five questions
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1.a) With the help of necessary sketches explain the potential distribution in an open circuited PN junction.
b) With the help of V-I Characteristics, explain the operation of a PN Diode under Forward bias and Reverse bias. [7+8]

2.a) With neat sketches explain the operation of a FWR with shunt capacitor filter & Derive the expression for its ripple factor.
b) A bridge rectifier uses four identical diodes having forward resistance of 5Ω each. Transformer secondary resistance is 5 ohms and the secondary voltage is 30V (rms). Determine the dc output voltage for I_{dc} = 200 mA and value of the output ripple voltage. [7+8]

3.a) Draw the circuit diagram of NPN transistor in Common Base (CB) configuration. With neat sketches and necessary equations, describe its static input- output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?
b) With reference to a BJT, define the following terms and explain:
i) Emitter efficiency.
ii) Base transportation factor.
iii) Large signal current gain. [9+6]

4.a) Obtain the condition for thermal stability of a BJT used in a biasing circuit?
b) Design a self bias circuit using silicon transistor to achieve a stability factor of 10, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50. [5+10]

5.a) Draw the circuit diagram & small signal equivalent circuit of CE amplifier using accurate h-parameter model. Derive expressions for A_V, A_I, R_i & R_0.
b) A bipolar junction transistor with h_{ie} = 1100Ω, h_{fe} = 50, h_{re} = $2.4x10^{-4}$, h_{oe} = 25 μA/V, is to drive a load of 1KΩ in Emitter-Follower arrangement. Estimate A_V, A_I, R_i & R_0? [8+7]

6.a) With the help of neat sketches and characteristic curves explain the construction & operation of a JFET and mark the regions of operation on the characteristics?
b) Show that in Field Effect Transistor, the transconductance, $g_m = g_{mo} [1- V_{GS}/ Vp]$ [8+7]

7.a) Draw the basic structure and equivalent circuit of UJT. Explain how the UJT can be used as a negative-resistance device with the aid of static characteristics**.**

b) In the common source FET amplifier shown in Figure.1, the transconductance and drain dynamic resistance of the FET are 5mA/V and 1MΩ respectively**.** Estimate A_V, R_i & R_0?

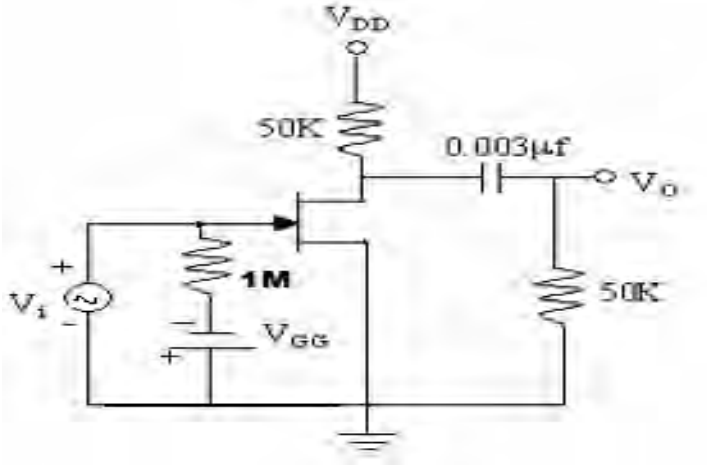

Figure.1

8.a) With neat sketches and necessary expressions describe V-I characteristics of a semiconductor photo diode?

b) With neat sketches and necessary expressions describe the operation of Varactor diode? [8+7]

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Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) Explain Avalanche and Zener break down mechanisms in semiconductors and compare them?

b) For the Zener diode circuit shown in Figure.1, determine V_L, V_R , I_Z & R. [5+10]

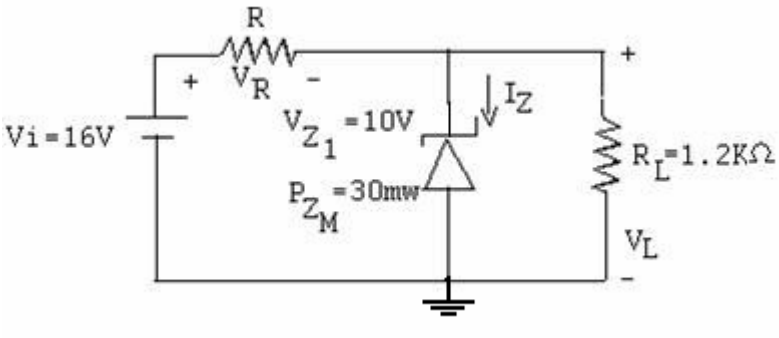

Figure.1

2.a) With reference to the Rectifiers, Explain the following terms:
i) Ripple Factor
ii) Efficiency
iii) Peak Inverse Voltage (PIV)
iv) % Regulation

b) A 230 V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in a full wave rectifier having a load of 900Ω. If the diode resistance and the secondary coil resistance together have a resistance of 100 Ω, determine
i) DC voltage across the load.
ii) DC current flowing through the load.
iii) DC power delivered to the load.
iv) PIV across each diode. [8+7]

3.a) Draw the circuit diagram of NPN transistor in Common Collector (CC) configuration. With neat sketches and necessary equations, describe its static input- output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?

b) Derive the relationship among α, β and γ in transistors? [9+6]

4.a) What do you mean by biasing a transistor? Explain the need of biasing a transistor for the construction of a faithful amplifier?

b) Design an Emitter bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: V_{CC} = 16V, V_{BE} = 0.7V, V_{CEQ} = 8V, I_{CQ} = 4 mA & β= 50. [7+8]

5.a) Draw the circuit and small-signal model of CE amplifier with unbypassed emitter resistor. Derive the expressions for input resistance & voltage gain?

b) A bipolar junction transistor with h_{ie} = 1100Ω, h_{fe} = 50, h_{re} = 2.4x10^{-4}, h_{oe} = 25 μA/V, is to drive a load of 1KΩ in CB amplifier arrangement. Estimate A_V, A_I, R_i & R_0. [8+7]

6.a) Explain the construction & operation of a N-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?

b) In an n-channel FET, the effective channel width is 3x 10^{-4}cm and the donor impurity concentration is 10^{15} electrons/cm^3. Find the pinch-off voltage? [10+5]

7.a) Show the self-bias arrangement for a Field Effect Transistor. With necessary expressions describe the procedure of Q-point establishment and stabilization?

b) In the common source FET amplifier shown in Figure.2, the transconductance and drain dynamic resistance of the FET are 5mA/V and 1MΩ respectively**.** Estimate A_V, R_i & R_0. [8+7]

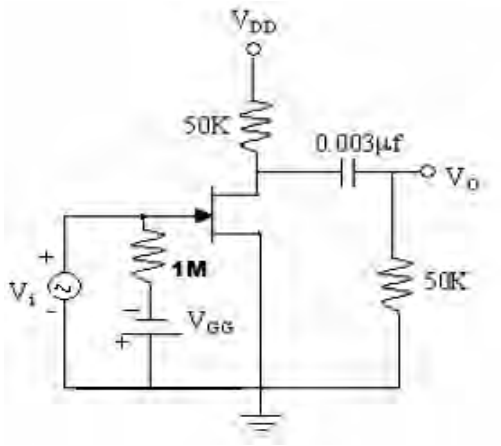

Figure.2

8.a) With neat energy band diagrams, explain the V-I characteristics of Tunnel diode. Also discuss the negative resistance property of tunnel diode.

b) Draw the two-transistor model of SCR and explain its operation. [10+5]

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